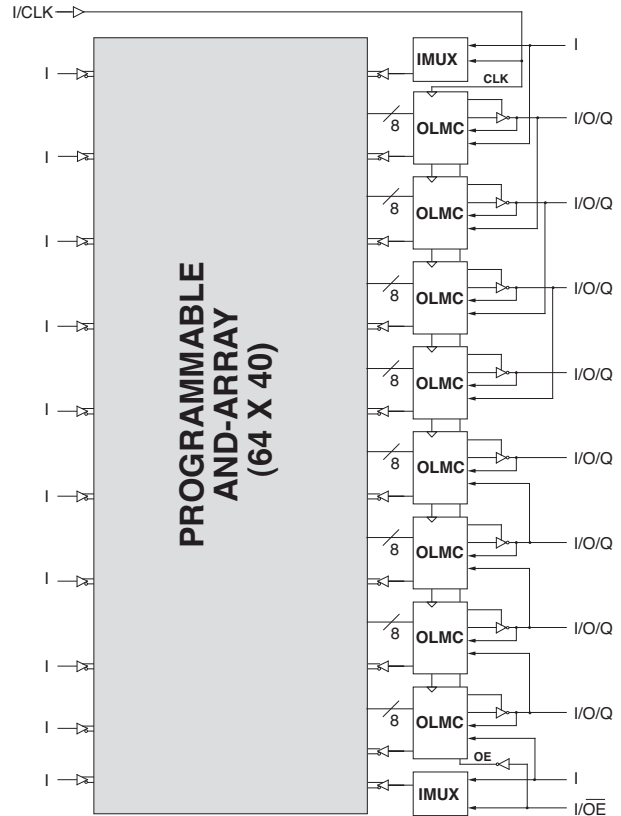


**Features**

- **HIGH PERFORMANCE E<sup>2</sup>CMOS® TECHNOLOGY**
  - 5 ns Maximum Propagation Delay
  - Fmax = 166 MHz
  - 4 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS**
- **E<sup>2</sup> CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 24-pin PAL® Devices with Full Function/ Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **LEAD-FREE PACKAGE OPTIONS**

**Functional Block Diagram**



Select devices have been discontinued. See Ordering Information section for product status.

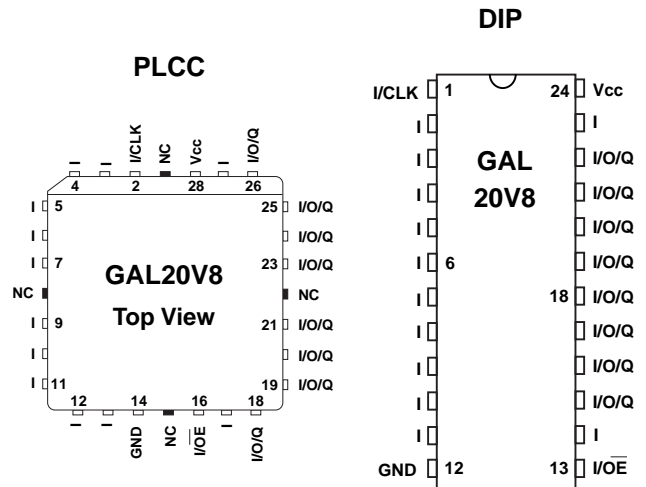
**Description**

The GAL20V8C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E<sup>2</sup>) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8 are the PAL architectures listed in the table of the macrocell description section. GAL20V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

**Pin Configuration**



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## Lead-Free Packaging Commercial Grade Specifications

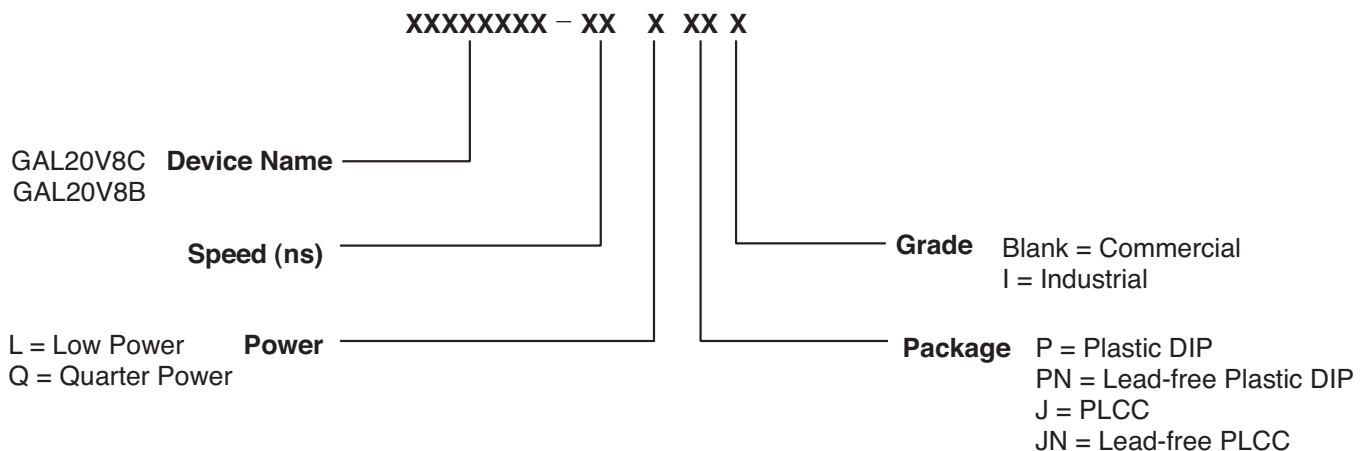
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJN <sup>1</sup>	Lead-Free 28-Lead PLCC
7.5	7	5	115	GAL20V8C-7LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-7LPN <sup>1</sup>	Lead-Free 24-Pin Plastic DIP
10	10	7	115	GAL20V8C-10LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-10LPN	Lead-Free 24-Pin Plastic DIP
15	12	10	55	GAL20V8B-15QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-15QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-15LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-15LPN	Lead-Free 24-Pin Plastic DIP
25	15	12	55	GAL20V8B-25QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-25QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-25LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-25LPN	Lead-Free 24-Pin Plastic DIP

## Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8C-10LJNI	Lead-Free 28-Pin Plastic DIP
			130	GAL20V8B-10LPNI <sup>1</sup>	Lead-Free 24-Pin Plastic DIP
15	12	10	130	GAL20V8B-15LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-15LPNI	Lead-Free 24-Pin Plastic DIP
20	13	11	65	GAL20V8B-20QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-20QPNI	Lead-Free 24-Pin Plastic DIP
25	15	12	65	GAL20V8B-25QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-25QPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL20V8B-25LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-25LPNI	Lead-Free 24-Pin Plastic DIP

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

## Part Number Description



Select devices have been discontinued. See Ordering Information section for product status.

## Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20V8 can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20V8	GAL20V8 Global OLMC Mode
20R8	Registered
20R6	Registered
20R4	Registered
20RP8	Registered
20RP6	Registered
20RP4	Registered
20L8	Complex
20H8	Complex
20P8	Complex
14L8	Simple
16L6	Simple
18L4	Simple
20L2	Simple
14H8	Simple
16H6	Simple
18H4	Simple
20H2	Simple
14P8	Simple
16P6	Simple
18P4	Simple
20P2	Simple

Select devices have been discontinued. See Ordering Information section for product status.

## Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 13 (DIP pinout) are permanently

configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 22 and pin 15 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins ( pins 18 and 19) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered" <sup>1</sup>	"Complex" <sup>1</sup>	"Simple" <sup>1</sup>	GAL20V8A
PLDesigner	P20V8R <sup>2</sup>	P20V8C <sup>2</sup>	P20V8C <sup>2</sup>	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS <sup>3</sup>	G20V8

1) Used with **Configuration** keyword.

2) Prior to Version 2.0 support.

3) Supported on Version 1.20 or later.

## Absolute Maximum Ratings<sup>(1)</sup>

Supply voltage  $V_{CC}$  ..... -0.5 to +7V  
 Input voltage applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Off-state output voltage applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Storage Temperature ..... -65 to 150°C  
 Ambient Temperature with

Power Applied ..... -55 to 125°C  
 1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## Recommended Operating Conditions

**Commercial Devices:**  
 Ambient Temperature ( $T_A$ ) ..... 0 to 75°C  
 Supply voltage ( $V_{CC}$ )  
 with Respect to Ground ..... +4.75 to +5.25V

**Industrial Devices:**  
 Ambient Temperature ( $T_A$ ) ..... -40 to 85°C  
 Supply voltage ( $V_{CC}$ )  
 with Respect to Ground ..... +4.50 to +5.50V

## DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>3</sup>	MAX.	UNITS
<b>V<sub>IL</sub></b>	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
<b>V<sub>IH</sub></b>	Input High Voltage		2.0	—	$V_{CC} + 1$	V
<b>I<sub>IL</sub><sup>1</sup></b>	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-100	μA
<b>I<sub>IH</sub></b>	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
<b>V<sub>OL</sub></b>	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
<b>V<sub>OH</sub></b>	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
<b>I<sub>OL</sub></b>	Low Level Output Current		—	—	24	mA
<b>I<sub>OH</sub></b>	High Level Output Current		—	—	-3.2	mA
<b>I<sub>OS</sub><sup>2</sup></b>	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA

### COMMERCIAL

I <sub>CC</sub>	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 15MHz Outputs Open	L -7/-10	—	75	115	mA
			L -15/-25	—	75	90	mA
			Q -15/-25	—	45	55	mA

### INDUSTRIAL

I <sub>CC</sub>	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 15MHz Outputs Open	L -10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

- 1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
- 2) One output at a time for a maximum duration of one second.  $V_{out} = 0.5V$  was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
- 3) Typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

Select devices have been discontinued. See Ordering Information section for product status.

## AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND <sup>1</sup> .	DESCRIPTION	COM		COM / IND		COM / IND		IND		COM / IND		UNITS
			-7		-10		-15		-20		-25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
<b>t<sub>pd</sub></b>	A	Input or I/O to 8 outputs switching	3	7.5	3	10	3	15	3	20	3	25	ns
		Comb. Output 1 output switching	—	7	—	—	—	—	—	—	—	—	ns
<b>t<sub>co</sub></b>	A	Clock to Output Delay	2	5	2	7	2	10	2	11	2	12	ns
<b>t<sub>cf</sub><sup>2</sup></b>	—	Clock to Feedback Delay	—	3	—	6	—	8	—	9	—	10	ns
<b>t<sub>su</sub></b>	—	Setup Time, Input or Fdbk before Clk ↑	7	—	10	—	12	—	13	—	15	—	ns
<b>t<sub>h</sub></b>	—	Hold Time, Input or Fdbk after Clk ↑	0	—	0	—	0	—	0	—	0	—	ns
<b>f<sub>max</sub><sup>3</sup></b>	A	Maximum Clock Frequency with External Feedback, 1/(t <sub>su</sub> + t <sub>co</sub> )	83.3	—	58.8	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t <sub>su</sub> + t <sub>cf</sub> )	100	—	62.5	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	62.5	—	62.5	—	50	—	41.7	—	MHz
<b>t<sub>wh</sub></b>	—	Clock Pulse Duration, High	5	—	8	—	8	—	10	—	12	—	ns
<b>t<sub>wl</sub></b>	—	Clock Pulse Duration, Low	5	—	8	—	8	—	10	—	12	—	ns
<b>t<sub>en</sub></b>	B	Input or I/O to Output Enabled	3	9	3	10	—	15	—	18	—	25	ns
	B	$\overline{OE}$ to Output Enabled	2	6	2	10	—	15	—	18	—	20	ns
<b>t<sub>dis</sub></b>	C	Input or I/O to Output Disabled	2	9	2	10	—	15	—	18	—	25	ns
	C	$\overline{OE}$ to Output Disabled	1.5	6	1.5	10	—	15	—	18	—	20	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from f<sub>max</sub> with internal feedback. Refer to **f<sub>max</sub> Descriptions** section.

3) Refer to **f<sub>max</sub> Descriptions** section.

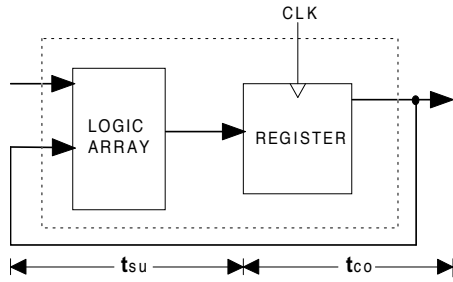
## Capacitance (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C <sub>i</sub>	Input Capacitance	8	pF	V <sub>CC</sub> = 5.0V, V <sub>I</sub> = 2.0V
C <sub>i/o</sub>	I/O Capacitance	8	pF	V <sub>CC</sub> = 5.0V, V <sub>I/O</sub> = 2.0V

\*Characterized but not 100% tested.

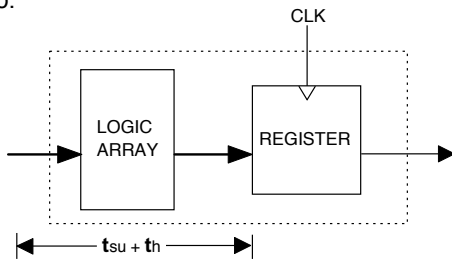
Select devices have been discontinued. See Ordering Information section for product status.

**f<sub>max</sub> Descriptions**



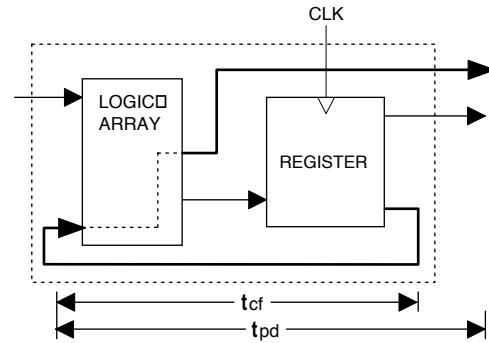
**f<sub>max</sub> with External Feedback 1/(tsu+tco)**

**Note:** f<sub>max</sub> with external feedback is calculated from measured tsu and tco.



**f<sub>max</sub> with No Feedback**

**Note:** f<sub>max</sub> with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



**f<sub>max</sub> with Internal Feedback 1/(tsu+tcf)**

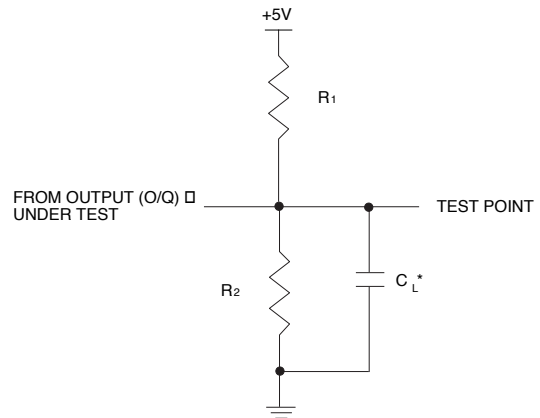
**Note:** tcf is a calculated value, derived by subtracting tsu from the period of f<sub>max</sub> w/internal feedback (tcf = 1/f<sub>max</sub> - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Select devices have been discontinued. See Ordering Information section for product status.

**Switching Test Conditions**

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL20V8B	2 – 3ns 10% – 90%
	GAL20V8C	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.



\*C<sub>L</sub> INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

**GAL20V8B Output Load Conditions (see figure)**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>
A	200Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	200Ω	390Ω
C	Active High	∞	390Ω
	Active Low	200Ω	390Ω

**GAL20V8C Output Load Conditions (see figure)**

Test Condition	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>
A	200Ω	200Ω	50pF
B	Active High	∞	200Ω
	Active Low	200Ω	200Ω
C	Active High	∞	200Ω
	Active Low	200Ω	200Ω